

JEDEC STANDARD

1.05 V CMOS

JESD8-34

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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1.05 V CMOS

(From JEDEC Board Ballot JCB-19-07, formulated under the cognizance of the JC-16 Committee on Interface Technology, Item 159.01.)

1 Scope

This standard defines the input, output specifications and ac test conditions for devices that are designed to operate narrow range 1.05 V CMOS level.

2 Standard specifications

All voltages are referenced to ground except where noted.

3 Electrical definitions

Table 1 1.05V CMOS input level specification

Item	Min/Max		Unit	Note
ViH	Min	0.8xVDD	V	
	Max	VDD+0.2	V	
ViL	Min	-0.2	V	
	Max	0.2xVDD	V	

4 DC operating Condition

Table 2 DC Operating Condition

Symbol	Min	Typ	Max	Unit	Note
VDD	1.01	1.05	1.12	V	



Standard Improvement Form

JEDEC

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

3. Other suggestions for document improvement:

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